REMARKS

The specification has been amended to correct a typographical error on page 2 (see the accompanying marked-up page).

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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integrated circuit becomes very high occurs. For solving the problem, Japanese Unexamined Patent Publication No. Hei 11(1999)-195976 (first literature) discloses a method of preparing a plurality of kinds of MOS transistors having different threshold voltages and selectively using the MOS transistors in accordance with the degree of timing allowance of a signal path in a semiconductor integrated circuit.

To address the request for reduction in power consumption, Japanese Unexamined Patent Publication No. Hei 10(1998)-189749 (U.S. Patent No. 6,093,043) (second literature) discloses a method of preparing a plurality of power supply voltages and selectively using a circuit for supplying a high voltage and a circuit for supplying a low voltage, thereby reducing the power.

The method disclosed in the first literature intends to achieve both improvement in operating speed and reduction in leak current in the standby mode by applying a circuit using a MOS transistor of a low threshold voltage to a path having no timing allowance (critical path) and applying a circuit using a MOS transistor having a high threshold voltage to other paths. In a circuit to which the technique is applied, however, when an attempt is made to reduce the power consumption in active operation by decreasing the power supply voltage, the threshold voltage of a MOS transistor has to be also decreased to maintain the operating speed. It was clarified by the examination of